

# Low Voltage Single Supply SPDT Analog Switch

## NL5S4599, NL5ST4599

The NL5S4599 and NL5ST4599 are advanced high speed CMOS single pole – double throw (SPDT) analog switches fabricated with silicon gate CMOS technology. These achieve high speed propagation delays and low ON resistances while maintaining low power dissipation. These switches control analog and digital voltages that may vary across the full power-supply range (from  $V_{CC}$  to GND).

These devices have been designed so the ON resistance ( $R_{ON}$ ) is much lower and more linear over the input voltage range than  $R_{ON}$  of typical CMOS analog switches.

The channel select input structures of these devices provide protection when voltages between 0 V and 5.5 V are applied, regardless of the supply voltage. These input structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

The NL5S4599 has CMOS level channel select input while the NL5ST4599 has TTL level channel select input.

### Features

- Channel Select Input Over-Voltage Tolerant to 5.5 V
- Fast Switching and Propagation Speeds
- Break-Before-Make Circuitry
- Low Power Dissipation:  $I_{CC} = 2 \mu A$  (Max) at  $T_A = 25 \text{ }^\circ C$
- Diode Protection Provided on Channel Select Input
- Improved Linearity and Lower ON Resistance Over Input Voltage
- ESD Performance: Human Body Model > 4000 V
- Chip Complexity: 38 FETs
- -Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS-Compliant

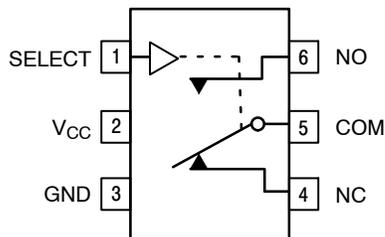


Figure 1. Pinout (Top View)

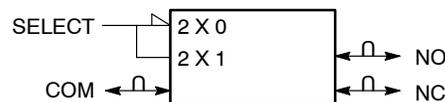
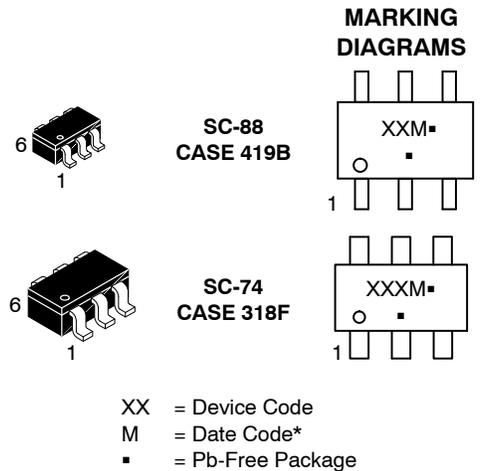


Figure 2. Logic Symbol



(Note: Microdot may be in either location)

\*Date Code orientation and/or position may vary depending upon manufacturing location.

### FUNCTION TABLE

Select	ON Channel
L	NC
H	NO

### ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 9 of this data sheet.

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## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit	
V <sub>CC</sub>	Supply Voltage	-0.5 to +6.5	V	
V <sub>IS</sub>	Analog I/O Voltage	-0.5 to V <sub>CC</sub> + 0.5	V	
V <sub>IN</sub>	Select Pin Voltage	-0.5 to +6.5	V	
I <sub>IN</sub>	DC Current, In or Out of Any Pin	±128	mA	
T <sub>STG</sub>	Storage Temperature Range	-65 to +150	°C	
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 secs	260	°C	
T <sub>J</sub>	Junction Temperature Under Bias	+150	°C	
θ <sub>JA</sub>	Thermal Resistance (Note 1)	SC-88 SC-74	377 320	°C/W
P <sub>D</sub>	Power Dissipation in Still Air at 25 °C	SC-88 SC-74	332 390	mW
MSL	Moisture Sensitivity	Level 1	-	
F <sub>R</sub>	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	-
V <sub>ESD</sub>	ESD Withstand Voltage (Note 2)	Human Body Model Charged Device Model	4000 2000	V
I <sub>LATCHUP</sub>	Latchup Performance (Note 3)		±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 10mm-by-1inch, 2 ounce copper trace no air flow per JESD51-7.
2. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.
3. Tested to EIA/JESD78 Class II.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	Supply Voltage	2.0	5.5	V
V <sub>IN</sub>	Select Input Voltage (Note 4)	0	5.5	V
V <sub>IS</sub>	Analog I/O Voltage (NC, CO, COM)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Free-Air Temperature	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Select Input Rise or Fall Time			ns/V
		V <sub>CC</sub> = 3.0 V to 3.6 V	0	100
		V <sub>CC</sub> = 4.5 V to 5.5 V	0	20

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Select input must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). It must not float.

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### DC ELECTRICAL CHARACTERISTICS – SELECT Input and Supply

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	Maximum			Unit
				-55 to 25 °C	<85 °C	<125 °C	

#### NL5S4599

V <sub>IH</sub>	Minimum High-Level Input Voltage, SELECT Input		2.0	1.5	1.5	1.5	V
			2.5	1.9	1.9	1.9	
			3.0	2.1	2.1	2.1	
			4.5	3.15	3.15	3.15	
			5.5	3.85	3.85	3.85	
V <sub>IL</sub>	Maximum Low-Level Input Voltage, SELECT Input		2.0	0.5	0.5	0.5	V
			2.5	0.6	0.6	0.6	
			3.0	0.9	0.9	0.9	
			4.5	1.35	1.35	1.35	
			5.5	1.65	1.65	1.65	

#### NL5ST4599

V <sub>IH</sub>	Minimum High-Level Input Voltage, SELECT Input		3.0	1.5	1.5	1.5	V
			4.5	2.0	2.0	2.0	
			5.5	2.0	2.0	2.0	
V <sub>IL</sub>	Maximum Low-Level Input Voltage, SELECT Input		3.0	0.5	0.5	0.5	V
			4.5	0.8	0.8	0.8	
			5.5	0.8	0.8	0.8	

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I <sub>IN</sub>	Maximum Input Leakage Current, SELECT Input	V <sub>IN</sub> = 5.5 V or GND	5.5	±0.1	±1.0	±1.0	μA
I <sub>OFF</sub>	Power Off Leakage Current, SELECT Input	V <sub>IN</sub> = 5.5 V or GND	0	±10	±10	±10	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current	V <sub>IN</sub> and V <sub>IS</sub> = V <sub>CC</sub> or GND	5.5	1.0	1.0	2.0	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

### DC ELECTRICAL CHARACTERISTICS – Analog

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	Maximum			Unit
				-55 to 25 °C	<85 °C	<125 °C	
R <sub>ON</sub>	Switch "ON" Resistance (Figures 17 – 23)	V <sub>IS</sub> = V <sub>CC</sub>  I <sub>IN</sub>   = 10.0 mA	2.5	85	95	105	Ω
			3.0	60	65	70	
			4.5	30	35	40	
			5.5	25	30	35	
R <sub>FLAT</sub>	ON Resistance Flatness (Figures 17 – 23)	V <sub>IS</sub> = V <sub>CC</sub>  I <sub>IN</sub>   = 10.0 mA	4.5	6	6	7	Ω
ΔR <sub>ON</sub>	ON Resistance Match Between Channels	V <sub>IS</sub> = 3.5 V  I <sub>IN</sub>   = 10.0 mA	4.5	4	4	5	Ω
I <sub>NC(OFF)</sub> I <sub>NO(OFF)</sub>	NO or NC Switch Off Leakage Current (Figure 9)	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>NO</sub> or V <sub>NC</sub> = 1.0 V V <sub>COM</sub> = 4.5 V	5.5	1	10	100	nA
I <sub>COM(ON)</sub>	NO or NC Switch ON Leakage Current (Figure 9)	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>NO</sub> = 1.0 V or 4.5 V with NC floating V <sub>NC</sub> = 1.0 V or 4.5 V with NO floating V <sub>COM</sub> = 1.0 V or 4.5 V	5.5	1	10	100	nA

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## AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	V <sub>IS</sub> (V)	-55 to 25 °C			<85 °C		<125 °C		Unit
					Min	Typ*	Max	Min	Max	Min	Max	
t <sub>ON</sub>	Turn-On Time (Figures 12, 13)	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF (Figures 5, 6)	2.5	2.0	5	13	28	5	30	5	30	ns
			3.0	2.0	5	11	21	5	25	5	25	
			4.5	3.0	2	9	16	2	20	2	20	
			5.5	3.0	2	8	14	2	20	2	20	
t <sub>OFF</sub>	Turn-Off Time (Figures 12, 13)	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF (Figures 5, 6)	2.5	2.0	1	7	12	1	15	1	15	ns
			3.0	2.0	1	7	10	1	15	1	15	
			4.5	3.0	1	6	9	1	12	1	12	
			5.5	3.0	1	6	8	1	12	1	12	
t <sub>BMM</sub>	Break-Before-Make Time	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF, V <sub>IS</sub> = 3.0 V (Figure 4)	2.5	2.0	1	7		1		1		ns
			3.0	2.0	1	5		1		1		
			4.5	3.0	1	4		1		1		
			5.5	3.0	1	4		1		1		

\*Typical Characteristics are at 25 °C.

## CAPACITANCE CHARACTERISTICS

Symbol	Parameter	Test Condition	V <sub>CC</sub> (V)	Typical (T <sub>A</sub> = 25 °C)	Unit
C <sub>IN</sub>	SELECT Input Capacitance		5.0	8	pF
C <sub>NO</sub> or C <sub>NC</sub>	Analog I/O (Switch OFF)		5.0	10	pF
C <sub>ON</sub>	Feedthrough (Switch ON)		5.0	26	pF
C <sub>COM</sub>	Common I/O		5.0	20	pF

## ADDITIONAL APPLICATION CHARACTERISTICS

Symbol	Parameter	Test Condition	V <sub>CC</sub> (V)	Typical (T <sub>A</sub> = 25 °C)	Unit
BW	ON-Channel -3 dB Bandwidth (Figure 10)	V <sub>IN</sub> = 0 dBm, V <sub>IN</sub> centered between V <sub>CC</sub> and GND (Figure 7)	3.0	170	MHz
			4.5	200	
			5.5	200	
V <sub>ONL</sub>	Feedthrough ON Loss	V <sub>IN</sub> = 0 dBm @ 100 kHz to 50 MHz, V <sub>IN</sub> centered between V <sub>CC</sub> and GND (Figure 7)	3.0	-3.0	dB
			4.5	-2.0	
			5.5	-2.0	
V <sub>ISO</sub>	Off-Channel Isolation (Figure 10)	f = 100 kHz, V <sub>IS</sub> = 1 V <sub>RMS</sub> , V <sub>IN</sub> centered between V <sub>CC</sub> and GND (Figure 7)	3.0	-93	dB
			4.5	-93	
			5.5	-93	
Q	Charge Injection, SELECT to Common I/O (Figure 15)	V <sub>IN</sub> = V <sub>CC</sub> to GND, f <sub>IS</sub> = 20 kHz, t <sub>r</sub> = t <sub>f</sub> = 3 ns, R <sub>IS</sub> = 0 Ω, C <sub>L</sub> = 1000 pF, Q = C <sub>L</sub> * ΔV <sub>OUT</sub> (Figure 8)	3.0	1.5	pC
			5.5	3.0	
THD+N	Total Harmonic Distortion + Noise (Figure 14)	f <sub>IS</sub> = 20 Hz to 100 kHz, R <sub>L</sub> = R <sub>gen</sub> = 600 Ω, C <sub>L</sub> = 50 pF, V <sub>IS</sub> = 5.0 V <sub>PP</sub> sine wave	5.5	0.1	%

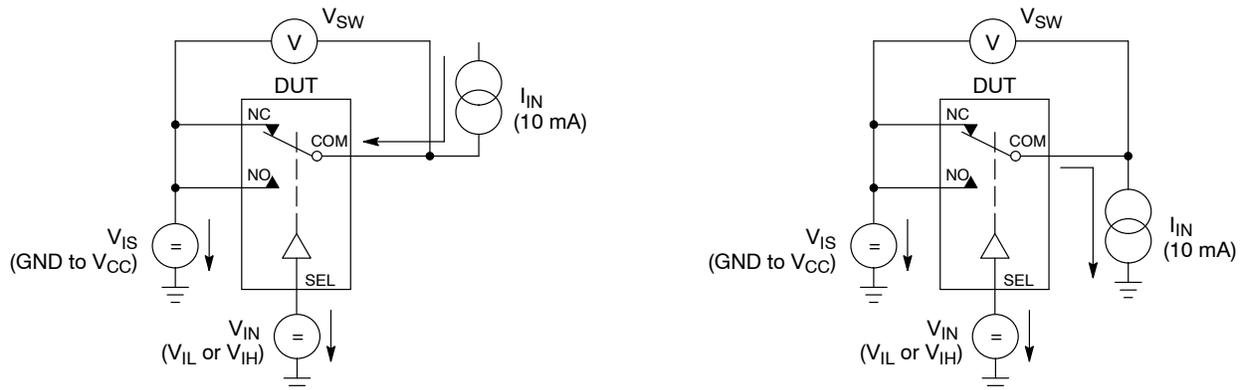


Figure 3. R<sub>ON</sub> (ON Resistance)

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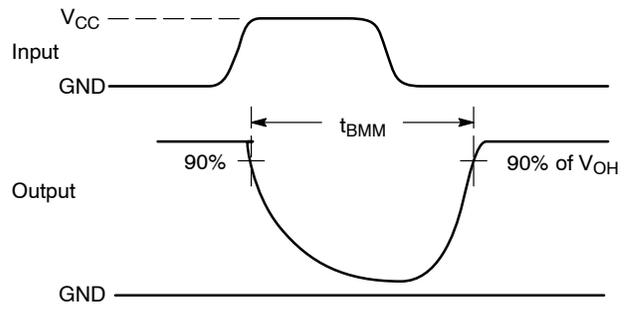
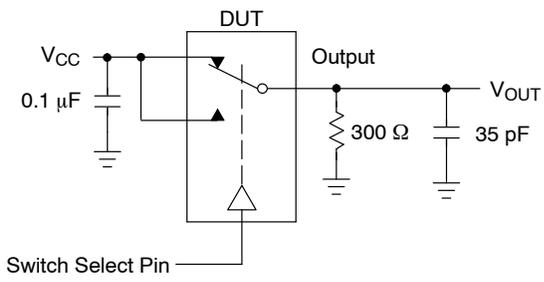


Figure 4.  $t_{BMM}$  (Break-Before-Make Time)

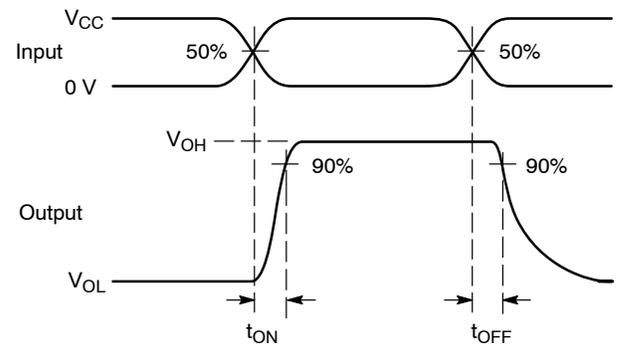
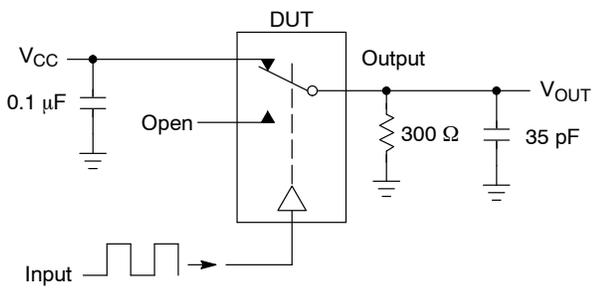


Figure 5.  $t_{ON}/t_{OFF}$

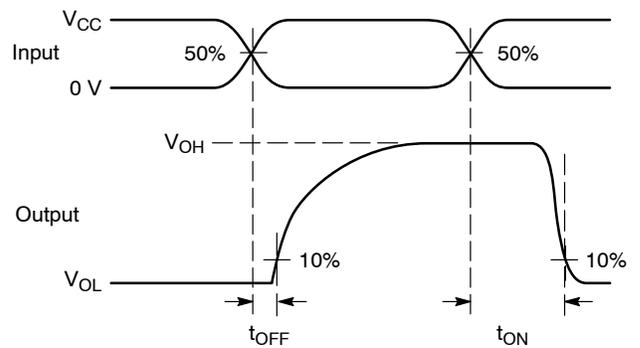
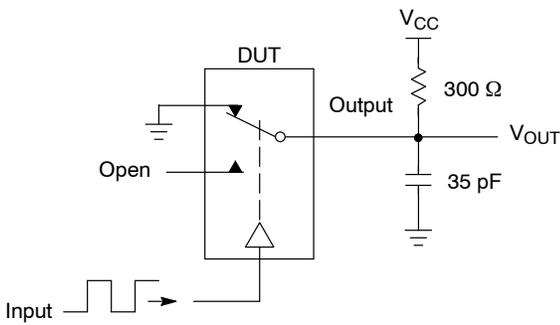
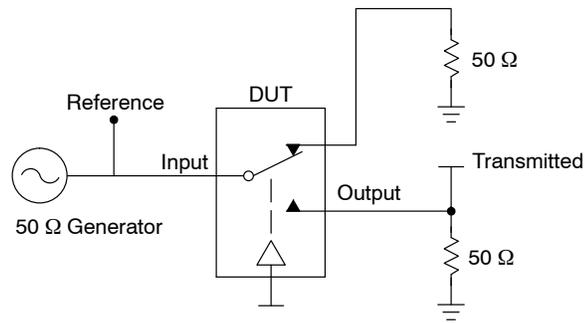


Figure 6.  $t_{ON}/t_{OFF}$

## NL5S4599, NL5ST4599



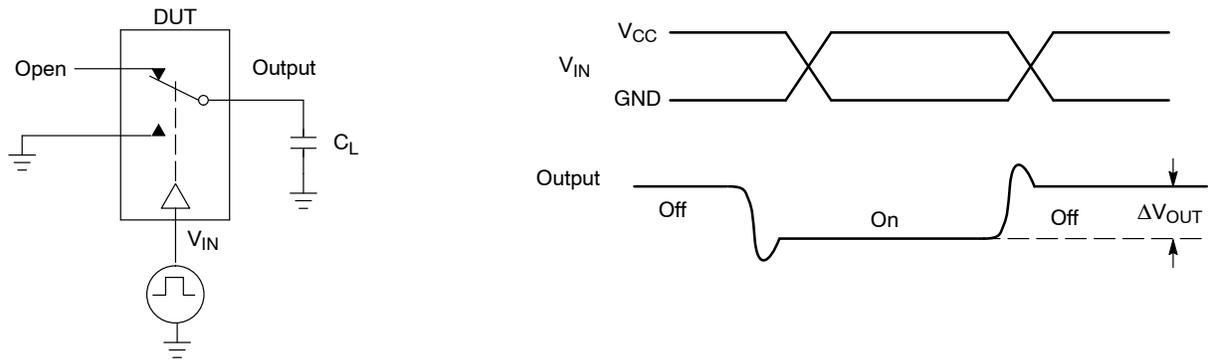
Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch.  $V_{ISO}$ , Bandwidth and  $V_{ONL}$  are independent of the input signal direction.

$$V_{ISO} = \text{Off Channel Isolation} = 20 \text{ Log} \left( \frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz}$$

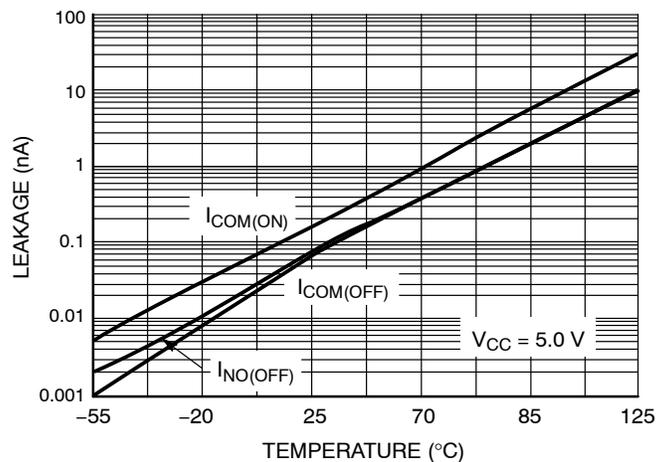
$$V_{ONL} = \text{On Channel Loss} = 20 \text{ Log} \left( \frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz to } 50 \text{ MHz}$$

Bandwidth (BW) = the frequency 3 dB below  $V_{ONL}$

**Figure 7.  $V_{ISO}$  /  $V_{ONL}$  / BW**

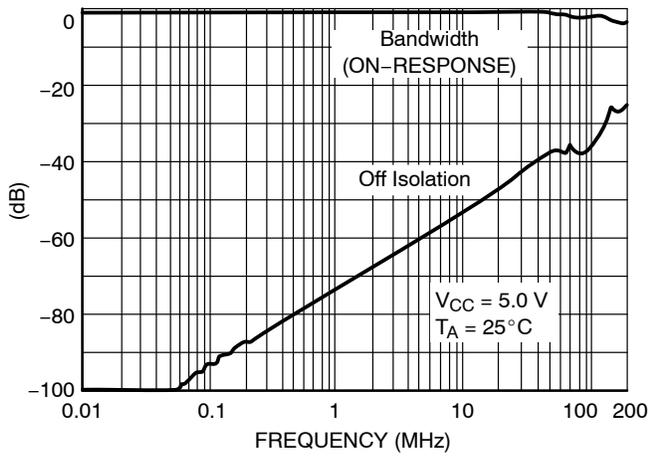


**Figure 8. Charge Injection**

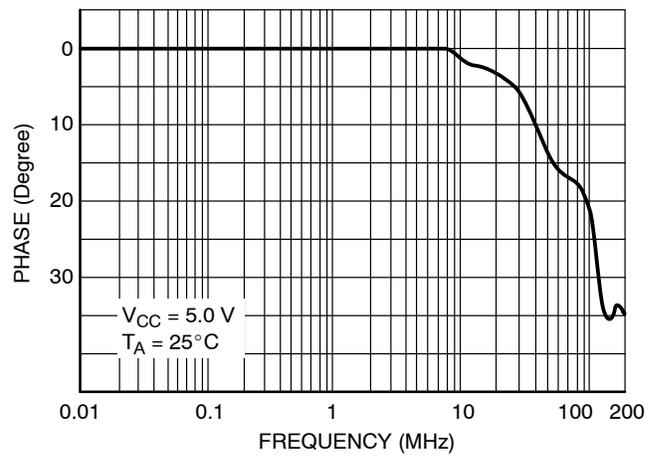


**Figure 9. Switch Leakage vs. Temperature**

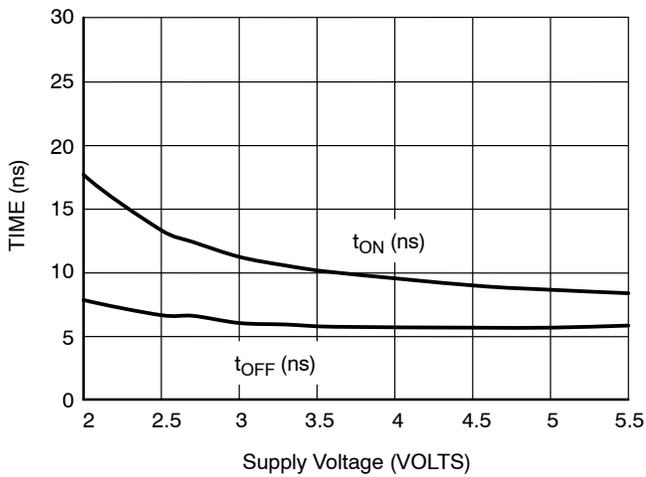
# NL5S4599, NL5ST4599



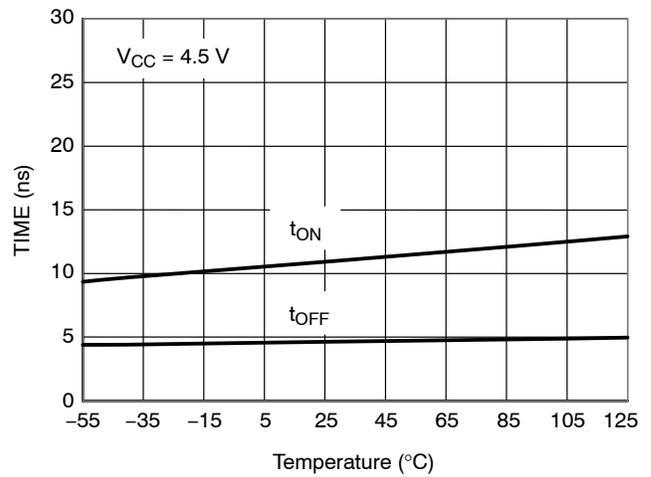
**Figure 10. Bandwidth and Off-Channel Isolation**



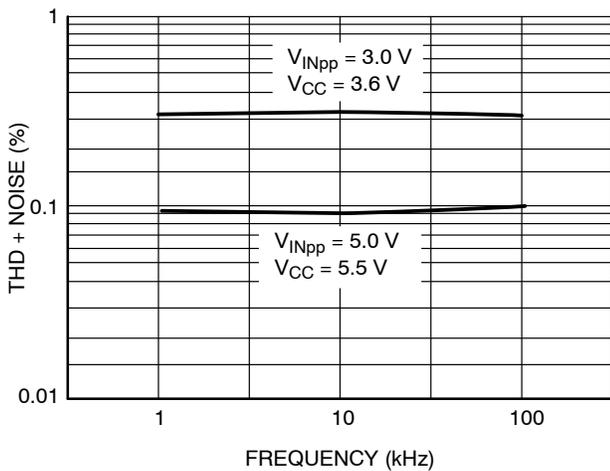
**Figure 11. Phase vs. Frequency**



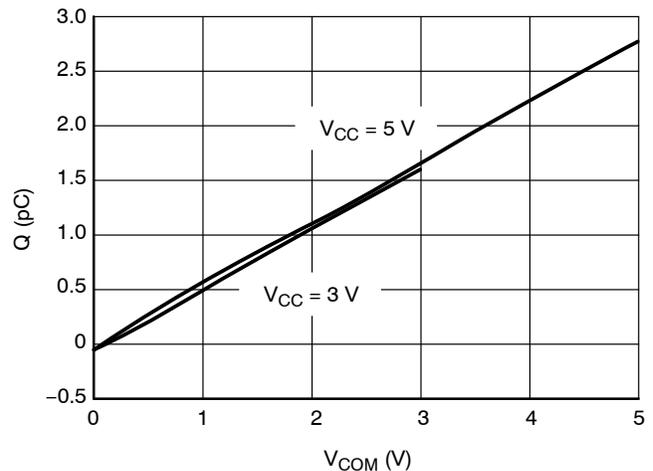
**Figure 12.  $t_{ON}$  and  $t_{OFF}$  vs.  $V_{CC}$  at 25 °C**



**Figure 13.  $t_{ON}$  and  $t_{OFF}$  vs. Temperature**



**Figure 14. Bandwidth and Off-Channel Isolation**



**Figure 15. Charge Injection vs. COM Voltage**

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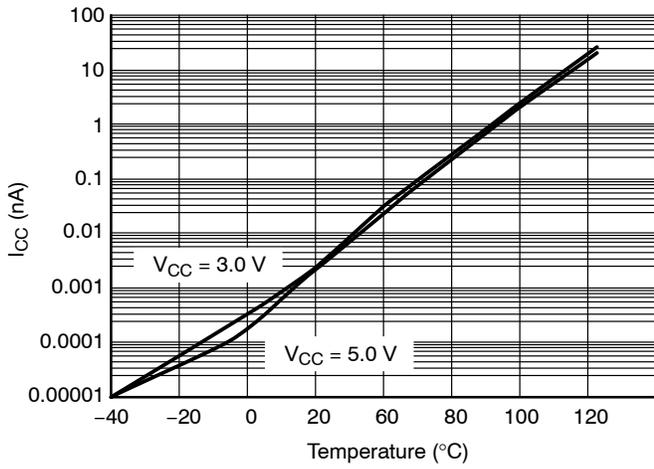


Figure 16.  $I_{CC}$  vs. Temp,  $V_{CC} = 3\text{ V}$  &  $5\text{ V}$

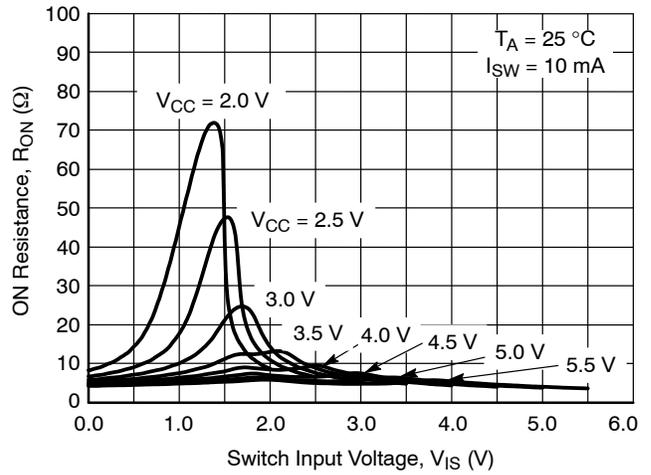


Figure 17.  $R_{ON}$  vs.  $V_{IS}$ ,  $T_A = 25^\circ\text{C}$

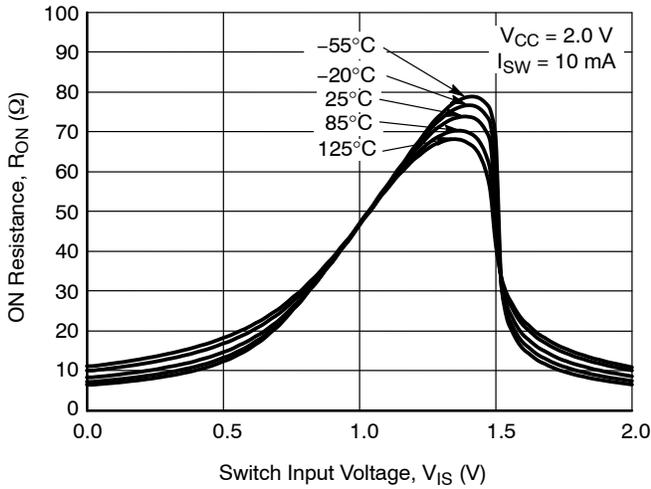


Figure 18.  $R_{ON}$  vs.  $V_{IS}$ ,  $V_{CC} = 2.0\text{ V}$

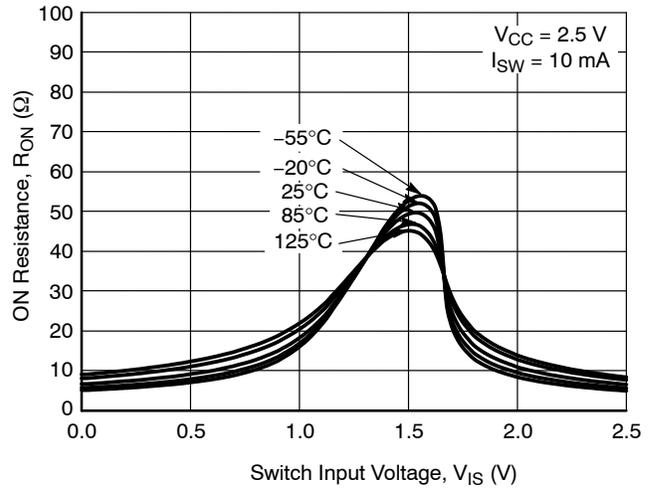


Figure 19.  $R_{ON}$  vs.  $V_{IS}$ ,  $V_{CC} = 2.5\text{ V}$

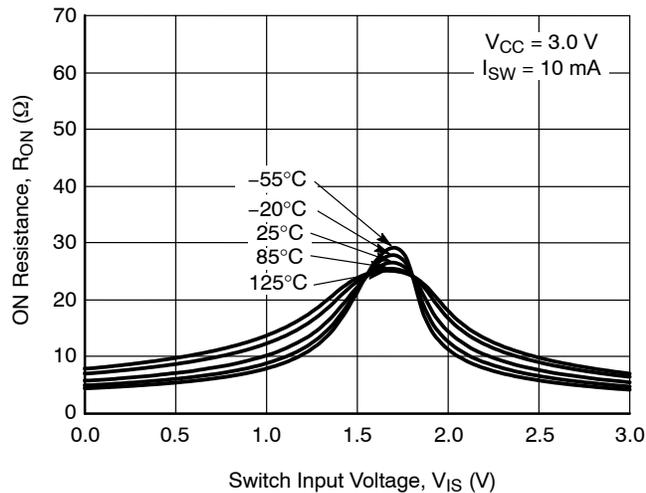


Figure 20.  $R_{ON}$  vs.  $V_{IS}$ ,  $V_{CC} = 3.0\text{ V}$

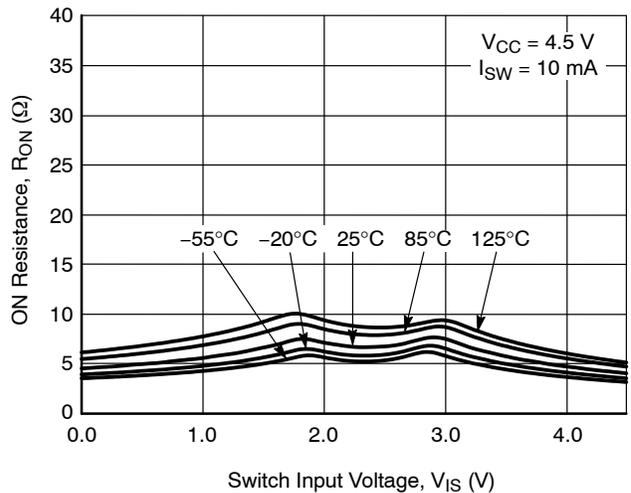


Figure 21.  $R_{ON}$  vs.  $V_{IS}$ ,  $V_{CC} = 4.5\text{ V}$

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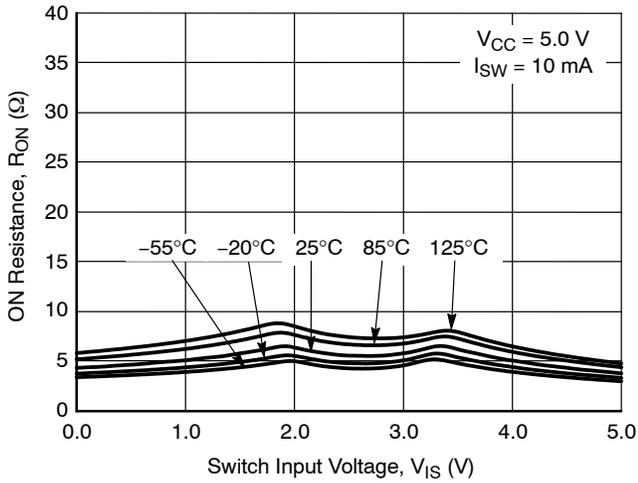


Figure 22.  $R_{ON}$  vs.  $V_{IS}$ ,  $V_{CC} = 5.0$  V

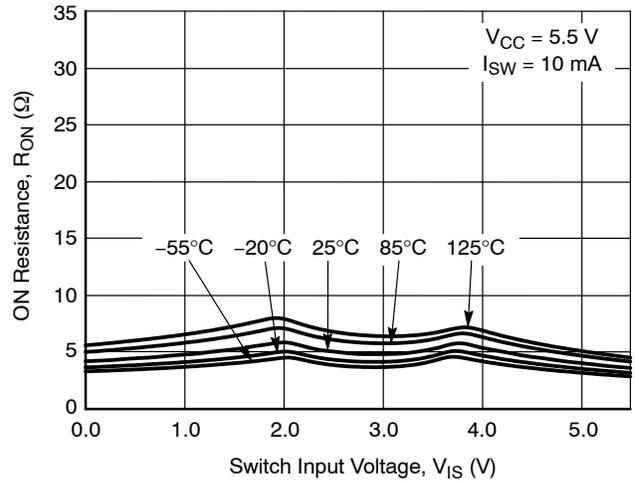


Figure 23.  $R_{ON}$  vs.  $V_{IS}$ ,  $V_{CC} = 5.5$  V

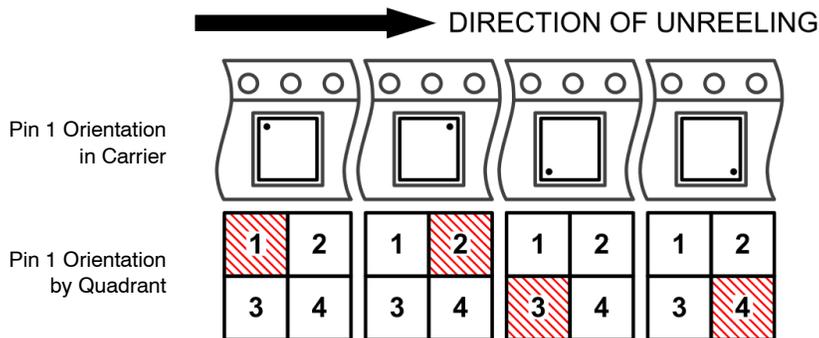
### ORDERING INFORMATION

Device	Package	Marking	Pin 1 Quadrant	Shipping <sup>†</sup>
NL5S4599DFT2G	SC-88	A2	3	3000 / Tape & Reel
NL5S4599DFT2G-Q*	SC-88	A2	3	3000 / Tape & Reel
NL5S4599DBVT1G	SC-74	A2	3	3000 / Tape & Reel
NL5S4599DBVT1G-Q*	SC-74	A2	3	3000 / Tape & Reel
NL5ST4599DFT2G	SC-88	A3	3	3000 / Tape & Reel
NL5ST4599DFT2G-Q*	SC-88	A3	3	3000 / Tape & Reel
NL5ST4599DBVT1G	SC-74	A3	3	3000 / Tape & Reel
NL5ST4599DBVT1G-Q*	SC-74	A3	3	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

\*-Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

### Pin 1 Orientation in Tape and Reel



### REVISION HISTORY

Revision	Description of Changes	Date
P0	Initial Preliminary Document release.	9/12/2025
P1	Corrected parameter and conditions text in DC table on page 3.	12/15/2025
0	Initial Document release.	2/10/2026

# NL5S4599, NL5ST4599

## PACKAGE DIMENSIONS

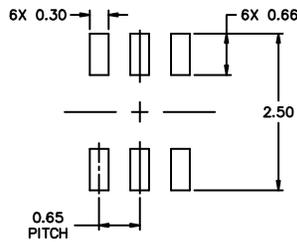
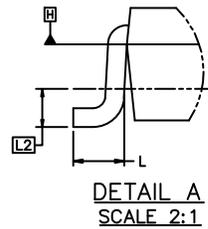
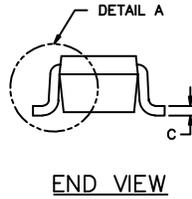
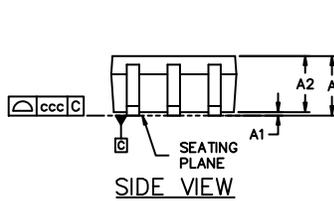
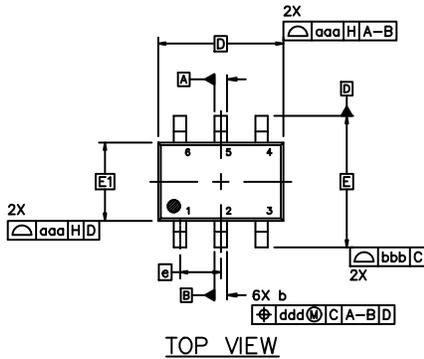
SC-88 2.00x1.25x0.90, 0.65P

CASE 419B-02

ISSUE Z

### NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.



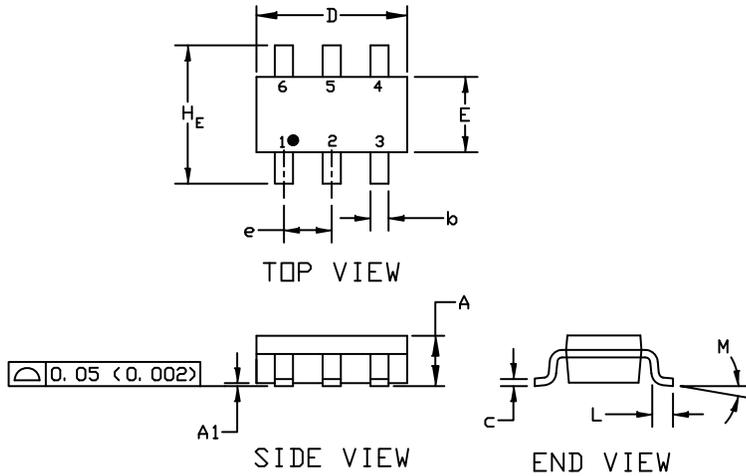
RECOMMENDED MOUNTING FOOTPRINT\*  
\* FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.00	---	0.10
A2	0.70	0.90	1.00
b	0.15	0.20	0.25
c	0.08	0.15	0.22
D	2.00 BSC		
E	2.10 BSC		
E1	1.25 BSC		
e	0.65 BSC		
L	0.26	0.36	0.46
L2	0.15 BSC		
aaa	0.15		
bbb	0.30		
ccc	0.10		
ddd	0.10		

# NL5S4599, NL5ST4599

## PACKAGE DIMENSIONS

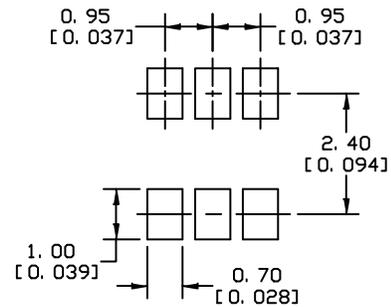
SC-74  
CASE 318F  
ISSUE P



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994
2. CONTROLLING DIMENSION: INCHES
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.

DIM	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.37	0.50	0.010	0.015	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
H <sub>E</sub>	2.50	2.75	3.00	0.099	0.108	0.118
L	0.20	0.40	0.60	0.008	0.016	0.024
M	0°	---	10°	0°	---	10°



\* For additional information on our Pb-Free strategy and soldering details, please download the DN Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

## SOLDERING FOOTPRINT

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